ESE 2025

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Main Examination

Electrical Engineering

Topicwise *Conventional* Solved Papers

Paper-II

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B. Singh (Ex. IES)

Director's Message

In past few years ESE Main exam has evolved as an examination designed to evaluate a candidate's subject knowledge. Studying engineering is one aspect but studying to crack prestigious ESE exam requires altogether different strategy, crystal clear concepts and rigorous practice of previous years' questions. ESE mains being conventional exam has subjective nature of questions, where an aspirant has to write elaborately - step by step with proper and well labeled diagrams and figures. This characteristic of the main exam gave me the aim and purpose to write this book. This book is an effort to cater all the difficulties being faced by students during their preparation right from conceptual clarity to answer writing approach.

MADE EASY Team has put sincere efforts in solving and preparing accurate and detailed explanation for all the previous years' questions in a coherent manner. Due emphasis is made to illustrate the ideal method and procedure of writing subjective answers. All the previous years' questions are segregated subject wise and further they have been categorised topic-wise for easy learning and helping aspirants to solve all previous years' questions of particular area at one place. This feature of the book will also help aspirants to develop understanding of important and frequently asked areas in the exam.

I would like to acknowledge the efforts of entire MADE EASY team who worked hard to solve previous years' questions with accuracy. I hope this book will stand upto the expectations of aspirants and my desire to serve the student community by providing best study material will get accomplished.

B. Singh (Ex. IES)
CMD, MADE EASY Group

ESE 2025
Main Examination

Electrical Engineering
Conventional Solved Questions

Paper-II

Contents

■■■■

1 Analog Electronics

Revised Syllabus of ESE: *Operational amplifiers – characteristics and applications.*

1. Operational Amplifier-Characteristics and Application

1.1 In an ideal operational amplifier, the voltage gain for the common mode signal is

(a) 0 (b) 0.5

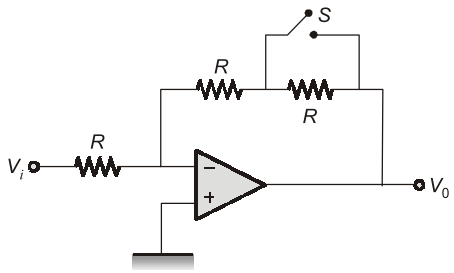
(c) 2.0 (d) infinite

[2 marks : 2002]

Solution: (a)

For an ideal operational amplifier, the voltage gain for the common mode signal is equal to zero.

1.2 The magnitude of the gain in the inverting operational amplifier circuit shown in figure is *Y*, with the switch open.



When the switch is closed the magnitude of the gain is

(a) $-Y$ (b) $Y/2$

(c) $2Y$ (d) $-2Y$

[2 marks : 2003]

Solution: (b)

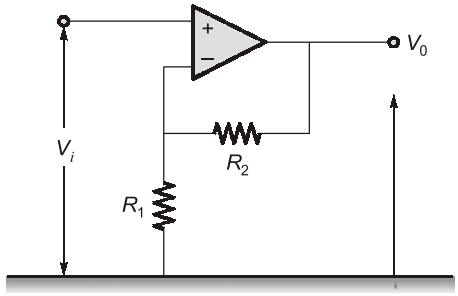
For inverting operational amplifier

$$V_0 = -\left(\frac{R_f}{R_1}\right)V_i$$

For switch is open, $$Y = \frac{V_0}{V_i} = -\left(\frac{2R}{R}\right) = -2$$

For switch is closed, $$Y' = \frac{V_0}{V_i} = -\left(\frac{R}{R}\right) = -1 = \left(\frac{Y}{2}\right)$$

1.3 The operational amplifier circuitry is given below. Determine its gain and indicate its applicability.

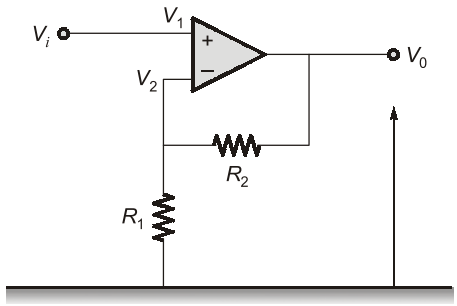


[7 marks : 2003]

Solution:

$$V_1 = V_i$$

and $$V_2 = \frac{V_0 \times R_1}{R_1 + R_2}$$



By virtual ground concept,

$$V_1 = V_2$$

$$\therefore \quad V_i = \frac{V_0 \times R_1}{R_1 + R_2}$$

$$\therefore \quad V_0 = \left(\frac{R_1 + R_2}{R_1}\right) V_i$$

Applications:

1. Used as comparator
2. As a zero crossing detector
3. Used as voltage follower circuit
4. Used in active peak detector
5. Used in rectifier circuit
6. Used in S-H circuit

1.4 Explain the operation of a Schmitt trigger circuit using an operational amplifier. Discuss the effect of hysteresis in such a circuit.

[8 marks : 2003]

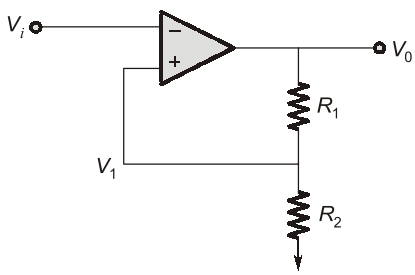
Solution:

Schmitt trigger or wave shaping circuit:

It is a switching circuit which converts non-rectangular wave form into rectangular waveform.

$$V_{UT} = \beta\, V_{sat} = \frac{R_2}{R_1 + R_2} V_0$$

$$V_{LT} = -\beta\, V_{sat} = \frac{-R_2}{R_1 + R_2} V_0$$



Schmitt trigger circuit:

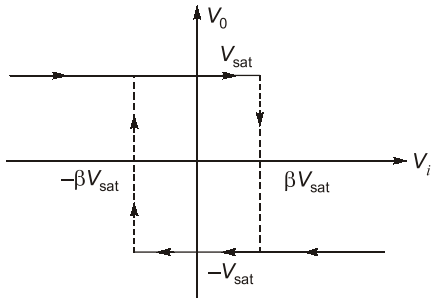
$$V_1 = \beta V_0$$

where, $$\beta = \frac{R_2}{R_1 + R_2}$$

Transfer characteristics of schmitt trigger exhibit hysteresis characteristics.

Let us consider voltage V_i is less than (V_1) we get the output of (+) $(V_{saturation})$ and if 'V_i' is increasing, then V_0 remains $(+V_{sat})$ until $(V_i = V_1)$, at this critical value, output voltage switches to $V_0 = (-V_{saturation})$ and remain at this value, as long as $(V_i > V_0)$.

The difference between V_{UT} and V_{LT} is defined as

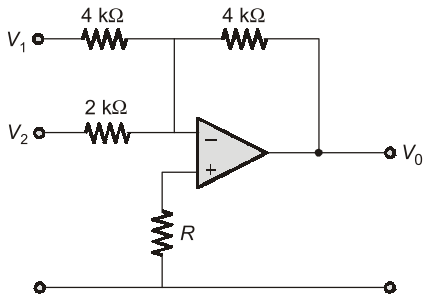


hysteresis V_H and given as

$$V_H = V_{UT} - V_{LT} = \frac{2R_2 V_0}{R_1 + R_2}$$

In such a circuit due to hysteresis loop, no transaction can takes place when $-\beta V_{sat} < V_i < \beta V_{sat}$

1.5 The most appropriate value of '*R*' in the circuit shown is



(a) 0 (b) 1 kΩ

(c) 2 kΩ (d) 4 kΩ [2 marks : 2004]

Solution: (a)

R is the dc resistance seen from the –ve terminal by removing all the sources by its internal resistance.

$\therefore \quad R = 2\ k\Omega \parallel 4\ k\Omega \parallel 4\ k\Omega = 1\ k\Omega$

1.6 The correct match between the pin numbers of an Op-Amp μA 741 in the left column and their functions in the right columns are

	Pin number		Functions
(A)	2	(P)	output
(B)	3	(Q)	non-inverting (+1 N)
(C)	4	(R)	inverting (–1 N)
(D)	6	(S)	$-V_{CC}$
		(T)	$+V_{CC}$

[5 marks : 2004]

Solution:

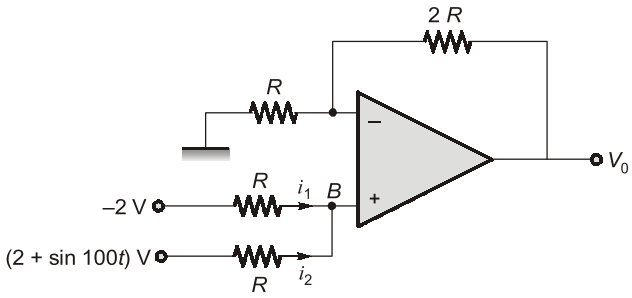
2 – (*R*) – inverting (–1 N)

3 – (*Q*) – non-inverting (+1 N)

4 – (*S*) – V_{CC}

6 – (*P*) – output

1.7 A non inverting operational amplifier summer is shown in the below figure. The output voltage V_0 is



(a) $\frac{3}{2}\sin 100t$ (b) $3\sin 100t$

(c) $\sin 100t$ (d) $2\sin 100t$

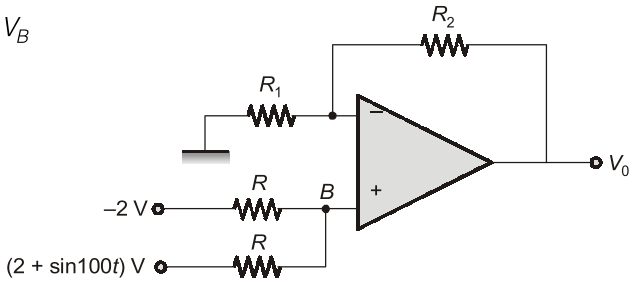
[2 marks : 2005]

Solution: (a)

$$R_2 = 2R$$
$$R_1 = R$$

According to concept of non-inverting amplifier

$$V_0 = V_B\left[1+\frac{R_2}{R_1}\right] = V\left(1+\frac{2R}{R}\right) = 3V_B$$



Now, $$V_B = -2\times\frac{R}{2R}+(2+\sin 100t)\times\frac{R}{2R}$$

$$= -1+1+\frac{\sin 100t}{2}$$

$$V_B = \frac{\sin 100t}{2}$$

$\therefore$ $$V_0 = 3V_B = \frac{3}{2}\sin 100t$$

1.8 Describe with necessary diagrams:

(i) an Integrator, and

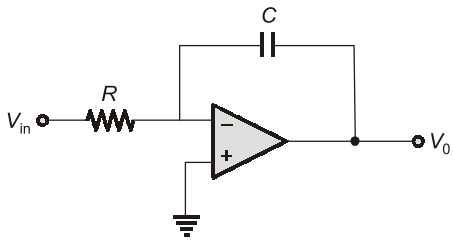
(ii) a differentiator using operational amplifier circuits. How the offset voltage can be minimized in an integrator at the output, and what is to be done to reset the integrator?
Discuss how in a practical differentiator high frequency oscillation can be prevented? How the outputs of a differentiator varies when (a) Ramp input is used, (b) Rectangular input is used?

[20 marks : 2005]

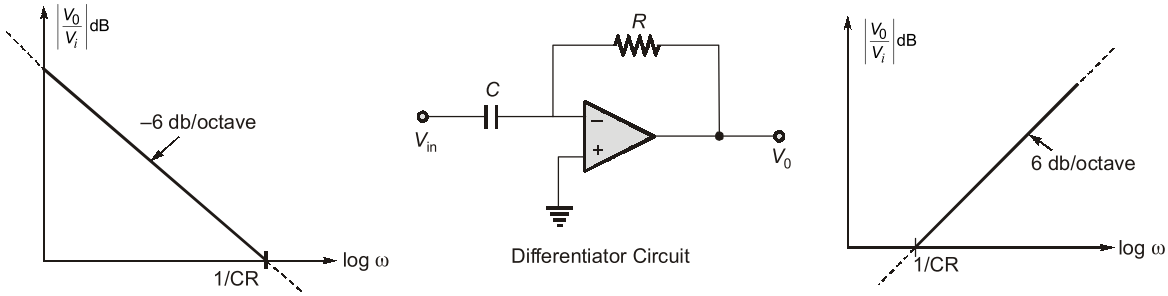
Solution:

$$V_0 = \frac{-1}{RCs}V_{in}$$

$\therefore$ $$V_0(t) = \frac{-1}{RC}\int V_{in}\,dt$$



Integrator circuit



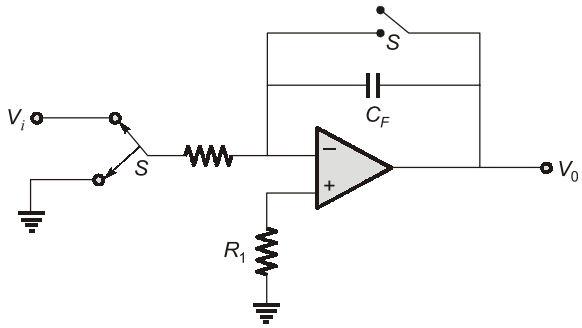
$$\therefore \quad V_0 = -RCs \times V_{in}$$

$$\therefore \quad V_0 = -RC\frac{d}{dt}V_{in}$$

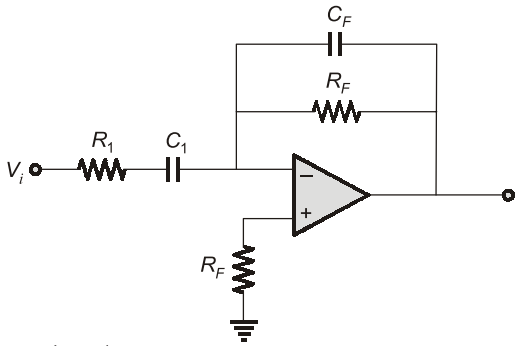
In integrator, feed back element is capacitor and thus at dc, where the capacitor behaves as an open circuit, there is no negative feedback. The offset voltage can be minimised using a resistance connected across the integrator capacitance *C*.

Practically we consider differentiator circuit as a 'noise magnifier. This is due to the spike introduced at the output every time there is a sharp change in $V_i(t)$.

For this reason it suffers stability problems. Otherwise for high frequency (ω_0), input applied to differentiator will get multiple of factor $-(RC\,\omega_0)$. Hence for a differentiator, level at the output increase immensely. We use an external circuit to reset the integrator as:



To eliminate the problem of high frequency oscillation in a differentiator circuit, circuit of differentiator is modified as:



and we take $R_1C_1 = R_FC_F$

For this we get, $f_b = \dfrac{1}{2\pi R_1C_1}$

So, till frequency f_b gain of differentiator increases but as frequency further increases above f_b, gain decreases at rate of –20 dB/decade so problem of instability at high frequency is solved.

(i) The output of the differentiator due to ramp input will be step signal.

$$r(t) = t$$

Output, $$c(t) = \frac{d}{dt}r(t) = u(t)$$

(ii) For a rectangular input,

$$r(t) = u(t) - u(t-T)$$

$$\therefore \quad \text{output} = \delta(t) - \delta(t-T)$$

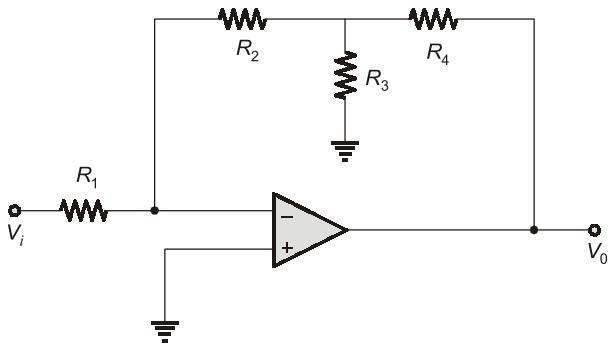
1.9 An operational Amplifier is basically a
(a) Low gain A.C. Amplifier
(b) High gain D.C. Amplifier
(c) High gain R.C. coupled Amplifier
(d) Low gain Transformer-coupled Amplifier

[2 marks : 2007]

Solution: (b)

An operational amplifier is basically a high gain DC amplifier.

1.10 Derive an expression for the closed loop gain V_0/V_i of the circuit shown below. Assume ideal Op-amp.



[10 marks : 2007]

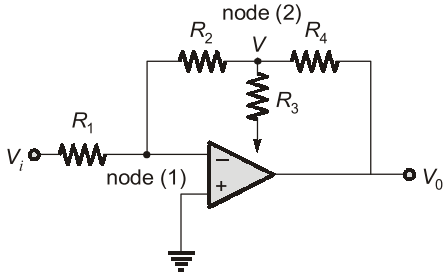
Solution:

By applying KCL at node (1)

By Virtual ground concept, voltage at node 1 = 0 V

$$\frac{0-V_i}{R_1}+\frac{0-V}{R_2} = 0$$

$$\therefore \quad V = -\left(\frac{R_2}{R_1}\right)V_i$$



Applying KCL on node 2,

$$\frac{V-0}{R_2}+\frac{V-V_0}{R_4}+\frac{V}{R_3} = 0$$

$$V\left(\frac{1}{R_2}+\frac{1}{R_4}+\frac{1}{R_3}\right) = \frac{V_0}{R_4}$$

$$V\left(\frac{R_3R_4+R_2R_3+R_2R_4}{R_2R_3R_4}\right) = \frac{V_0}{R_4}$$

Putting value of V_i in above expression,

$$\frac{-R_2}{R_1}\left(\frac{R_3R_4+R_2R_3+R_2R_4}{R_2R_3R_4}\right)\times R_4 = \frac{V_0}{V_i}$$

$$\therefore \quad \left(\frac{V_0}{V_i}\right) = \frac{-\left(R_3R_4+R_2R_3+R_2R_4\right)}{R_1R_3}$$

1.11 (i) Draw a single-stage, double-ended, transistorized differential amplifier and define offset and drift. What are the measures taken to minimize offset and drift?

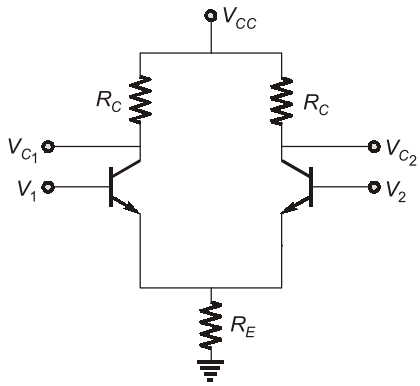
(ii) Sketch a single-stage, R.C. coupled, transistorized, common-emitter amplifier using npn transistor. Draw its frequency response. Why the gain is low at very low and very high frequencies? How the bandwidth of the amplifier is determined from this response?

[8 + 7 = 15 marks : 2007]

Solution:

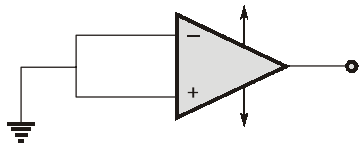
(i) Basic building block of op-amp [differential amplifier]

Common mode gain of the amplifier depends upon the value of (R_E), where R_E increases, common mode gain will decrease.

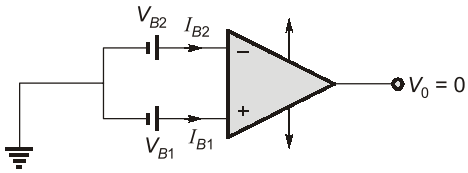


Terminology:

1. **Input offset voltage:** It is that voltage, which must be applied between the input to balance the amplifiers to get output voltage zero.
2. **Input offset current:** It is defined as the two biasing current entering the input terminal of the balanced amplifier.
3. **Input bias current:** It is the average of two bias current flowing into the two input terminal of the balanced amplifier.
4. **Output offset voltage:** It is the voltage at the output terminal, when the two input terminals are grounded.



V_{00} - output offset voltage because transistor are not identical



V_{i0} = (Input offset voltage) = $V_{B1} - V_{B2}$

Input offset current = $I_{i0} = I_{B1} - I_{B2}$, input bias current = $\frac{I_{B1} + I_{B2}}{2}$.

Offset: Shift in values of voltages and current in practical circuit with respect to ideal case is called offset voltage or current. To minimize the effect of offset voltages we add some additional voltage sources in circuit.

Similarly to minimize the effect of input offset current on output we introduce a resistance at +ve terminal whose value is equal to dc resistance seen from the –ve terminal by replacing all the sources by their internal impedances.

Drift: Change in bias current, offset current, and offset voltages due to change in temperature is called drift.

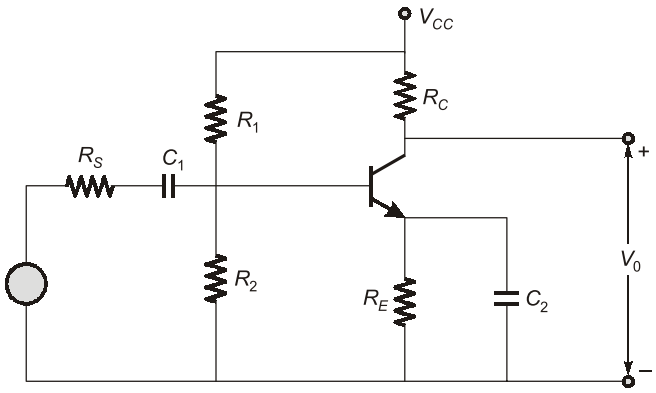
Offset current drift is expressed as μA/°C.

Offset voltage drift is expressed as μV/°C.

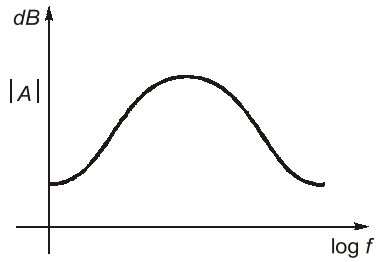
Careful printed circular boards are used to keep op-amps away from heat sources to minimize the problem of drift.

Sometimes forced cooling is also used to minimize the effect.

(ii)



Single-staged *RC* coupled common-emitter amplifier



Because of degeneration caused by 'R_E', the gain is low at very low and at very high frequency.

$$\text{Bandwidth} = f_H = \frac{0.35}{t_r}$$

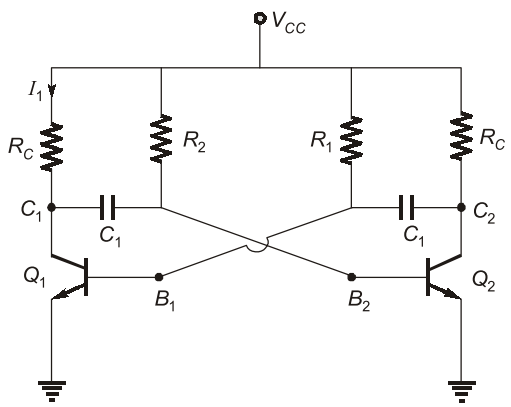
Where 't_r' is rise time of the circuit. Gain is low at low frequencies due to voltage drop across coupling and bypass capacitors. Gain is low at high frequencies because of internal junction capacitances which has finite impedance at high frequencies.

1.12 Draw the circuit diagram of a transistorzed collector-coupled astable multivibrator and explain the generation of square wave. In a symmetrical collector-coupled astable multivibrator $R_1 = R_2 = 1\ \text{M}\Omega$ and $C_1 = C_2 = 0.01\ \mu\text{F}$ find the frequency of operation.

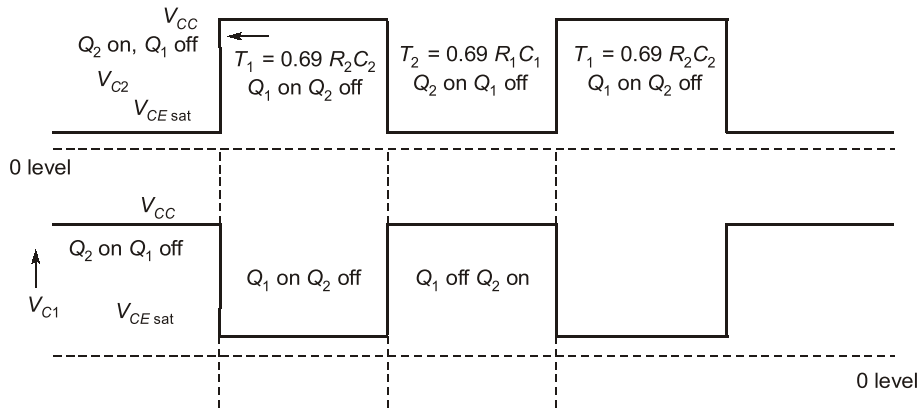
[10 marks : 2007]

Solution:

Circuit diagram:



Waveform will be as



We consider immediately before $t = 0$, transistor Q_2 is in saturation and Q_1 is below cutoff. Hence for $t < 0$, $V_{c2} = V_{CE\,sat}$ (low output) and $V_{c1} = V_{cc}$ (high output).

Now capacitor C_1 will charge through R_1 and transistor Q_2 and voltage V_B, start increasing, when V_{B1} reaches cut-in voltage V_γ, Q_1 starts conducting and draws a large current I_1 so that V_{c1} immediately falls to $V_{CE\,sat}$ so that V_{B2} also falls by amount I_1R_C and $V_{B2} < V_\gamma$ so Q_2 goes in cutoff and voltage V_{c2} suddenly rises to V_{CC}. This charging and discharging of capacitor continuous and conduction transfers from one transistor to another transistor after a certain time as to produce square wave (duty cycle may or may not be 50%).

We know that, $T_1 = 0.69R_2C_2$

$T_2 = 0.69R_1C_1$

Now given that, $R_1 = R_2 = 1\ \text{M}\Omega = 10^6\ \Omega = R$

$C_1 = C_2 = 0.01\ \mu F = 10^{-8}\ F = C$

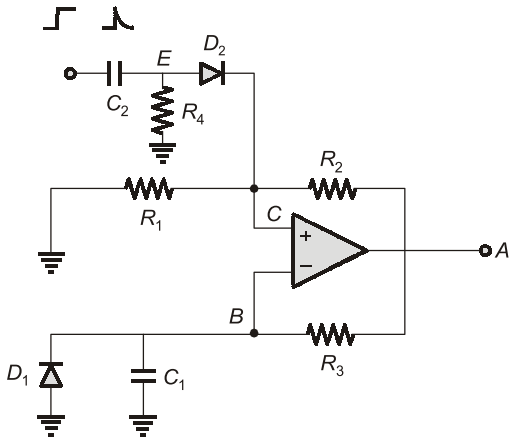
$\therefore$ Time period, $T = T_1 + T_2 = 0.69\,(R_1C_1 + R_2C_1) = 0.69 \times 2\,RC = 1.38\,RC$

$\therefore$ $$f = \frac{1}{T} = \frac{1}{1.38\,\text{RC}} = \frac{1}{1.38 \times 10^6 \times 10^{-8}} = \frac{100}{1.38}\,\text{Hz}$$

1.13 A monostable multivibrator is to be constructed using an OP-AMP. Draw the diagram generating a positive pulse and explain its working with the help of waveforms. Derive an expression for the period of the pulse in terms of the circuit parameters.

[16 marks : 2009]

Solution:



An OP-AMP monostable circuit:

Monostable multivibrator has one stable state and the other is quasi stable state. The circuit is useful for generating signal output pulse of adjustable time duration in response to triggering signal. The width of the pulse depends only on external components connected to the OP-AMP.

To analyse the circuit, let us assume that in the stable state, the output voltage is at $-V_{sat}$ [For getting positive pulse]. The diode 'D_1' conducts and 'V_B' the voltage across the capacitor 'C' gets clamped to (–0.7 V). The voltage at the positive input terminal through R_1 R_2 potentiometric divider is $-\beta V_{sat}$ or $[\beta L^{(-)}]$. Now if a trigger of magnitude 'V_i' is applied to the positive input terminal is greater than (–0.7 V).

$\therefore$ The output of the OP-AMP will switch from $-V_{sat}$ or $L^{(-)}$ to V_{sat} or $L^{(+)}$. The diode gets reverse biased and the capacitor starts charging exponentially to $(+V_{sat})$ through the resistance (R_3). When capacitor voltage (V_B) becomes just slightly more positive than $(+\beta\, V_{sat})$ or $(\beta\, L^{+})$, the output of the OP-AMP switches back to $-V_{sat}$. The capacitor 'C', now starts charging to $-V_{sat}$ or $-L^{(-)}$ through R_3 until V_B is (–0.7 V) as capacitor (C_1) gets clamped to the voltage. We observe that a five pulse is generated at the output during the quasi-stable state. The duration T of the output pulse is determined from the exponential waveform of V_B.

$$V_B(t) = L_+ - (L_+ - V_{D1})e^{-t/C_1R_3}$$

By substituting, $V_B(t) = \beta L_+$

$$\beta L_+ = L_+ - (L_+ - V_{D1})e^{-T/C_1R_3}$$

which yields,

$$T = C_1R_3 \ln\left(\frac{V_{D1} - L_+}{\beta L_+ - L_+}\right)$$

for $|V_{D1}| << |L_+|$ this equation is approximately

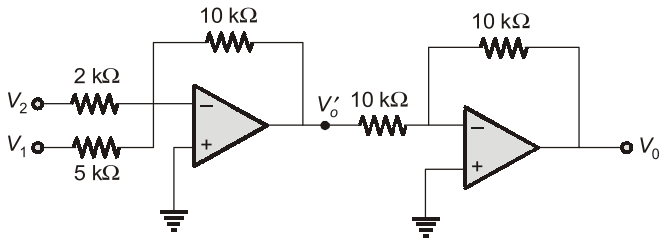
$$T \cong C_1R_3 \ln\left[\frac{1}{1-\beta}\right]$$

1.14 Design a circuit using minimum number of OA to realize the equation:

$$V_0 = 2V_1 + 5V_2$$

[10 marks : 2012]

Solution:



The output of first (OA) will be

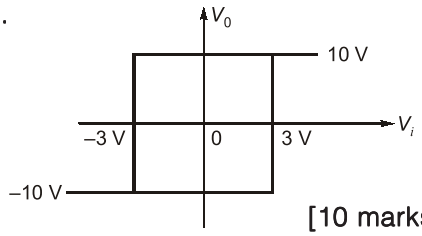
$$V_0' = -\left(\frac{10}{2}V_2 + \frac{10}{5}V_1\right) = -(5V_2 + 2V_1)$$

The second OA will acts as inverter,

$$V_0 = -\frac{10}{10}V_0'$$

$\therefore$ $$V_0 = 2V_1 + 5V_2$$

1.15 A circuit has the following voltage transfer characteristic. Design a circuit to realize this characteristic.



Plot the waveforms for V_0 when

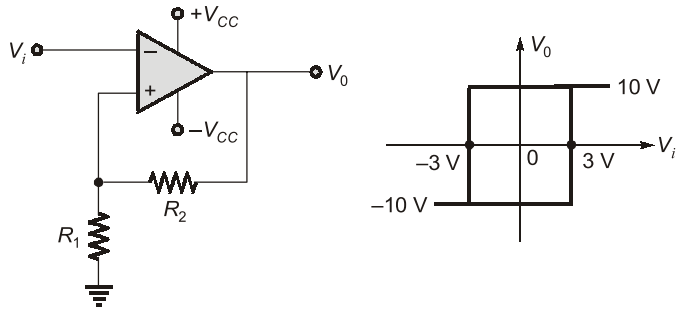
(i) $V_i = 5 \sin\omega t$

(ii) V_i = Half-wave rectified of 5 sinωt

[10 marks : 2012]

Solution:

Circuit for the given voltage transfer characteristic.



From given transfer characteristic,

Upper trip point (UTP) = 3 V

$$\frac{R_1}{R_1 + R_2} V_{sat} = 3 \text{ V}$$

and $V_{sat} = 10$ V

$$\therefore \quad \frac{R_1}{R_1 + R_2} = \frac{3}{10}$$

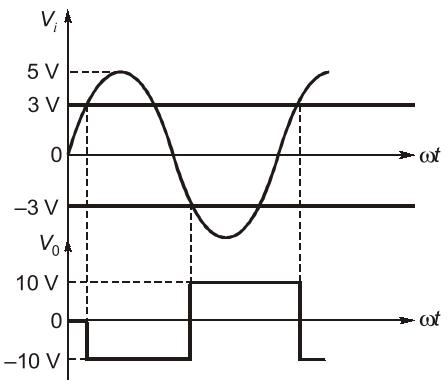
$$\Rightarrow \quad 1 + \frac{R_2}{R_1} = \frac{10}{3}$$

$$\frac{R_1}{R_2} = \frac{3}{7}$$

We can choose $R_1 = 3\,\text{k}\Omega$ and $R_2 = 7\,\text{k}\Omega$

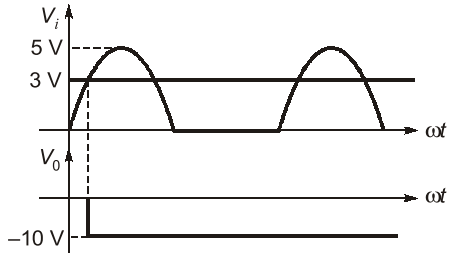
(i) When, $V_i = 5 \sin\omega t$

When the input voltage exceeds the UTP on the upward swing of the positive half cycle, the output voltage switches to $-V_{sat}$. Half a cycle latter, the input voltage become more negative than the LTP, and the output switches back to $+V_{sat}$.

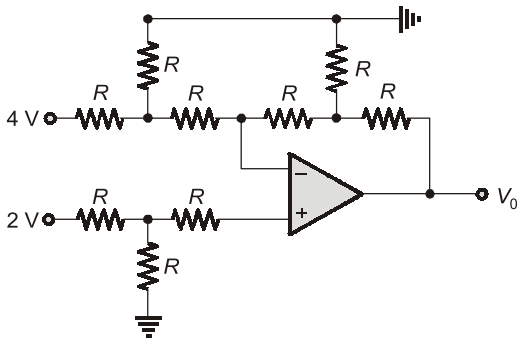


(ii) When V_i = half-wave rectified of 5 sinωt

As the input voltage will never become more negative then LTP, the output will never switch back to $+V_{sat}$.



1.16 Determine the output voltage V_0 of the circuit shown in the figure.



[10 marks : 2012]

Solution:

Applying KCL for V_1,

$$\frac{V_1-2}{R}+\frac{V_1}{R}+\frac{V_1-V}{R}=0$$

$$\Rightarrow \quad 3V_1 = 2 + V$$

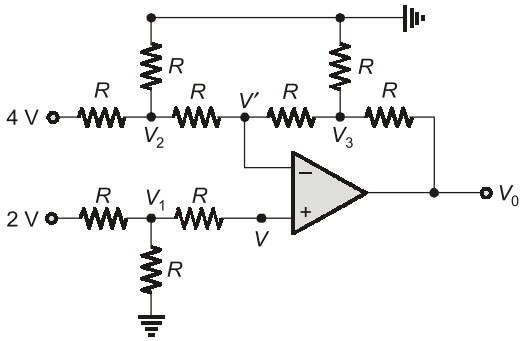
Since, no current flows into the op-amp,

$$V_1 = V$$

$$\therefore \quad 2V = 2$$

$$\Rightarrow \quad V = 1\text{ V} \qquad ...(1)$$

Also, due to internal short, $V' = V = 1$ V



Applying KCL for V_2,

$$\frac{V_2-4}{R}+\frac{V_2}{R}+\frac{V_2-1}{R}=0$$

$$3V_2 = 5$$

$$\Rightarrow \quad V_2 = \frac{5}{3}\text{ V} \qquad ...(2)$$

Applying KCL at node voltage V',

$$\frac{V'-V_2}{R}+\frac{V'-V_s}{R}=0$$

$$2V' = V_2 + V_3$$

$$\Rightarrow \quad V_3 = 2-\frac{5}{3}$$

$$V_3 = \frac{1}{3}\text{ V} \qquad ...(3)$$

Now, applying KCL and node V_s,

$$\frac{V_3 - 1}{R} + \frac{V_s}{R} + \frac{V_3 - V_0}{R} = 0$$

$$V = 3V_3 - 1 = 0 \text{ V}$$

1.17 **Define slew rate and PSRR of an operational amplifier. Explain clearly the difference between Bandwidth, transient response and slew-rate of an op-amp.**

[4 marks : 2013]

Solution:

Slew rate: It is defined as the maximum rate of change of output voltage per unit of time and is expressed as volt per micro second. An ideal op-amp has infinite slew rate.

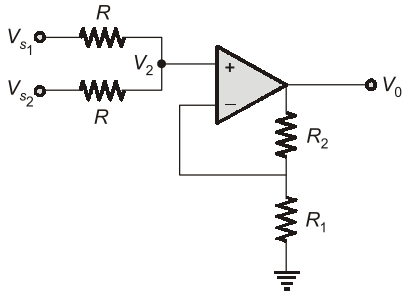
PSRR: The PSRR is defined as the ratio of the change in supply voltage to the equivalent (differential) input voltage it produces in the op-amp, often expressed in decibles. An ideal op-amp has infinite PSRR.

$$\text{PSRR} = \frac{\Delta V_{\text{supply}}}{\Delta V_{IOS}}$$

Bandwidth: It is the range of frequency for which amplifier can faithfully amplify the signal.

Transient Response: When the system is subjected to an input, the output tries to reach to steady state value. This process of achieving steady state value is called transient response.

1.18 **Find an expression for the output V_0 of the amplifier circuit shown below. Assume an ideal op-amp. What mathematical operation does the circuit perform?**



[4 marks : 2013]

Solution:

$$V_2 = \frac{V_{s_1} + V_{s_2}}{2}$$

By virtual ground theory, $V_2 = V_A$

$$V_2 = \frac{V_{s_1} + V_{s_2}}{2} = V_A$$

$$V_A = \left(\frac{R_1}{R_1 + R_2}\right) V_o$$

$$\Rightarrow \quad V_0 = \left(\frac{V_{s_1} + V_{s_2}}{2}\right)\left(\frac{R_2 + R_1}{R_1}\right)$$

$$\Rightarrow \quad V_0 = \left(\frac{V_{s_1} + V_{s_2}}{2}\right)\left(1 + \frac{R_2}{R_1}\right)$$

If $R_1 = R_2 = R$

$$\Rightarrow \quad V_0 = V_{s_1} + V_{s_2}$$

So mathematical operation performed is addition.